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EXAMINER	
NGUYEN, LAUREN	

ART UNIT	PAPER NUMBER
2871	

NOTIFICATION DATE	DELIVERY MODE
10/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/669,371	SONG, IN DUK	
	Examiner	Art Unit	
	LAUREN NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *7-9,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-16 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 07/09/2008 have been fully considered but they are not persuasive.

2. The applicant argues (see page 13) regarding the amended **claims 1, 12, 21** that Kim discloses a COG type and the data lines 620 and ground lines 700 are not located in a corner of the outer area of the picture display part. This is irrelevant and not persuasive. Kim may disclose a COG type but Kim's line-on glass type signal lines 620 are lines on glass, since the substrate is made of glass. In addition, since both of the lines 620 and 700 extend to the corners of the lower substrate, they are located in a corner of the outer area of the picture display part.

3. The applicant argues (see page 13) regarding the amended **claims 1, 12, 21** that **Moon** discloses that the second common voltage pads 143 are on the side of the panel 120. The examiner respectfully disagrees. Moon (figure 7) clearly shows the pad 143 is located at the corner of the outer area of the picture display part.

4. Applicant's arguments with respect to **claims 1-6, 10-16, 19-23** have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> a. A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 21-22** are rejected under 35 U.S.C. 102(b) as being anticipated by **Moon et al. (US 2002/0044246)**.

7. Regarding **claim 21**, **Moon et al.** (figure 7) discloses a line-on glass liquid crystal display panel, comprising:

- a picture display part (127) with a matrix of liquid crystal cells having a plurality of gate lines (132) and date lines (134) to cross each other;
- a gate pad and a data pad (150 and 124) to drive the gate lines., and data lines, respectively;
- a plurality of line-on glass type signal lines (138) located in one comer of an outer area of the picture display part of a lower substrate for applying drive signals to drive the liquid crystal cells; and
- a plurality of dummy lines (128B) that formed between gate signal lines,
- wherein the plurality of dummy lines are a common voltage line or a ground voltage line.

Please note that the claims are directed to apparatus which must be distinguished over the prior art in term of structure rather than functions [MPEP 2114]. Hence, the functional limitations of *"for applying a common voltage a reference voltage to drive the liquid crystal cell"* which are narrative in form have not been given any patentable weight. In order to be given patentable weight, a functional recitation must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. See In re Danley, 120 USPQ 528, 531 (CCPA 1959).

8. Regarding **claim 22**, **Moon et al.** (figure 7) implicitly discloses the gate signal lines are Vgl, Vet, Vgh, GOE, GSC, CISP.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-6, 12-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Moon et al. (US 2002/0044246)** in view of **Kim et al. (KR 10-1999-0024956)**.

11. Regarding **claim 1**, **Moon et al.** (figure 7) discloses a line-on glass liquid crystal display panel, comprising:

- a picture display part having liquid crystal cells at each intersection of gate lines and data lines (132 and 134);
- data pads (124) extended from the data lines (134) in an outer area of the picture display part (127);
- gate pads (150) extended from the gate lines (132) in the outer area of the picture display part (127);
- a first and a second line-on glass signal pads (136, 140) near to an end of the data pads and an end of the gate pads, respectively, in one comer of the outer area of the picture display part;
- a plurality of line-on glass type signal lines (138) connecting the first and second line-on glass signal pads (136, 140) in the comer of the outer area of the picture display part for applying gate power voltage signals and gate control signals to gate drive lCs in order to drive gate signal lines of the picture display part; and
- at least one dummy line (128B) formed between the line-on glass type signal lines (138) for applying a common voltage a reference voltage to drive the liquid crystal cell.

Please note that the claims are directed to apparatus which must be distinguished over the prior art in term of structure rather than functions [MPEP 2114]. Hence, the functional limitations of "*for applying gate power voltage signals and gate control signals to gate drive ICs in order to*

drive gate signal lines of the picture display part" and "for applying a common voltage a reference voltage to drive the liquid crystal cell" which are narrative in form have not been given any patentable weight. In order to be given patentable weight, a functional recitation must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. See In re Danley, 120 USPQ 528, 531 (CCPA 1959).

12. **Moon et al.** discloses the limitations as shown in the rejection of **claim 1** above. However, **Moon et al.** is silent regarding forming the insulating layer. **Kim et al.** (in at least paragraph 22, figures 1, 3-4, 6) teaches the insulating film (640) covers the plurality of line-on glass type signal lines (620 or 621) and the dummy line (700) is formed on the layer of the insulating film. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the insulating film as taught by **Kim et al.** because such modification would reduce the EMI effect and the wireless frequency interference.

13. Regarding **claim 2**, **Moon et al.** (figure 7) discloses the first and second line-on glass signal pads (136 and 140) which extend from both sides of the line-on glass type signal lines (138) and are respectively formed between the end of the gate pads and the end of the data pads (150 and 124).

14. Regarding **claim 3**, **Moon et al.** (figure 7) discloses first and a second dummy pads (122 and 143) that extend from both sides of the dummy line (128B) between the gate pads and the data pads (150 and 124).

15. Regarding **claim 4**, **Moon et al.** (figure 7) discloses the first and second dummy pads (122 and 143) are located between the first and second line-on glass type signal pads (136 and 140).

16. Regarding **claim 5**, **Kim et al.** (figures 1, 3-4, 6) discloses the line-on glass type signal lines (620) are formed in a same layer as the gate line (621) of the picture display part.

17. Regarding **claim 6, Kim et al.** (figures 1, 3-4, 6) discloses the dummy line (700) is formed in a same layer as a data line (621, figure 4) of the picture display part with a gate insulating film therebetween (640).

18. Regarding **claim 12, Moon et al.** (figure 7) discloses a fabricating method of a line-on glass liquid crystal display panel, comprising:

- forming gate lines (132) in a picture display part (127) and a plurality of line-on glass signal lines (138) in one corner of an outer area of the picture display part on a substrate for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part;
- forming data lines (134) to cross the gate lines in a picture display part and a dummy line that is located between the line-on glass signal lines for applying a common voltage as a reference voltage; and
- forming data pads (124) extended from the data lines and gate pads (150) extended from the gate lines in the outer area of the picture display part and forming first and second line-on glass signal pads (136 and 140) near to the data pads and gate pads, respectively, in one comer of the outer area of the picture display part,
- wherein the first and the second line-on glass signal pads (136 and 140) are connecting to the plurality of the line-on glass signal lines (138).

19. **Moon et al.** discloses the limitations as shown in the rejection of **claim 12** above. However, **Moon et al.** is silent regarding forming the insulating layer. **Kim et al.** (in at least paragraph 22, figures 1, 3-4, 6) teaches forming at least one layer of insulating film (640) to cover the line-on glass type signal lines (620 or 621) and a dummy line (700) that is located on the

insulating film. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the insulating film as taught by **Kim et al.** because such modification would reduce the EMI effect and the wireless frequency interference.

Please note that the claims are directed to apparatus which must be distinguished over the prior art in term of structure rather than functions [MPEP 2114]. Hence, the functional limitations of "*for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part" and "for applying a common voltage as a reference voltage"* which are narrative in form have not been given any patentable weight. In order to be given patentable weight, a functional recitation must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. See In re Danley, 120 USPQ 528, 531 (CCPA 1959).

20. Regarding **claim 13**, **Kim et al.** (figures 1, 3-4, 6) discloses forming a gate electrode connected to the gate line of the picture display part on the substrate; forming a gate insulating film (660) on the substrate on which the gate line and the gate electrode are formed; forming a semiconductor layer on the gate insulating film; forming a source electrode connected to the data line, and a drain electrode opposite to the source electrode with a designated gap therebetween (630), on the substrate on which the semiconductor is formed; forming a protective film (640) on the substrate where the data line, the source electrode and the drain electrode are formed; and forming a pixel electrode (650) connected to the drain electrode on the protective film.

21. Regarding **claim 14**, **Kim et al.** (figures 1, 3-4, 6) discloses the line-on glass signal line is formed of a same metal as a gate line (62').

22. Regarding **claim 15**, **Kim et al.** (figures 1, 3-4, 6) discloses the dummy line is formed of a same metal as the data line (700 and 621).

23. Regarding **claim 16**, **Kim et al.** (figures 1, 3-4, 6) discloses the dummy line (700) is formed between the line-on glass type signal lines (620) with the gate insulating film therebetween (640).

24. Claims 19-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon et al. (US 2002/0044246) in view of Song et al. (US 2002/0008794).

25. Regarding **claim 19, Moon et al.** (figure 7) discloses a line-on glass liquid crystal display panel, comprising:

- a picture display part (127) with a matrix of liquid crystal cells having a plurality of gate lines (132) and date lines (134) to cross each other;
- a gate pad and a data pad (150 and 124) to drive the gate lines and data lines, respectively;
- a plurality of line-on glass type signal lines (138) located in one comer of an outer area of the picture display part of a lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one comer of the outer area of the picture display part is corresponding to between the gate pad and the data pad; and
- a plurality of common voltage signal lines (128A and 128B) for applying a common voltage signal and being formed between gate signal lines.

26. **Moon et al.** discloses the limitations as shown in the rejection of **claim 19** above. However, **Moon et al.** is silent regarding forming the silver dot. **Song et al.** (in at least paragraph 0014, figure 4) teaches at least one of the plurality of common voltage lines applies the common voltage signal through a silver(Ag) dot (63) to a common electrode that is formed on an entire surface of an upper substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the silver dot as taught by **Song et al.** because such modification would provide an electrical connection with the common electrode of the upper substrate.

27. Regarding **claim 20**, **Moon et al.** (figure 7) implicitly discloses the gate signal lines are Vgl, Vet, Vgh, C.rOE, GSC, GSP.

28. Regarding **claim 23**, **Moon et al.** discloses the limitations as shown in the rejection of **claim 21** above. However, **Moon et al.** is silent regarding forming the silver dot. **Song et al.** (in at least paragraph 0014, figure 4) teaches at least one of the plurality of common voltage lines applies the common voltage signal through a silver(Ag) dot (63) to a common electrode that is formed on an entire surface of an upper substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the silver dot as taught by **Song et al.** because such modification would provide an electrical connection with the common electrode of the upper substrate.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lauren Nguyen whose telephone number is (571) 270-1428. The examiner can normally be reached on M-F, 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. N./
Examiner, Art Unit 2871

/Andrew Schechter/
Primary Examiner, Art Unit 2871